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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,385	12/06/2001	Jan Bernkopf	003424.P034	2212

8791 7590 10/07/2003

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EXAMINER	
PERRY, ANTHONY T	

ART UNIT	PAPER NUMBER
2879	

DATE MAILED: 10/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application N .	Applicant(s)	
	10/020,385	BERNKOPF, JAN	
	Examiner	Art Unit	
	Anthony T Perry	2879	

-- The MAILING DATE of this communication appears n the cover sheet with the correspondenc address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-31 and 33-44* is/are rejected.

7)☒ Claim(s) *8,10,20-22,30,32,42-44* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

Claims 8 and 30 are objected to because of the following informalities: replace "if" with --is--. Appropriate correction is required.

Claims 20-22 are objected to because claim 20 claims dependency from claim 9 while the drawings and specification teach otherwise. A pressure sensitive conductive layer that includes conducting and nonconducting regions is not shown to be used in conjunction with an insulating layer with a plurality of vias. Therefore, the Examiner has treated the claims as being dependent from base claim 1.

Claim 21 is objected to because of the following informalities: in line 2, replace "pattering" with --patterning--. Appropriate correction is required.

Claims 42-44 are objected to because claim 42 claims dependency from claim 31 while the drawings and specification teach otherwise. A pressure sensitive conductive layer that includes conducting and nonconducting regions is not shown to be used in conjunction with an insulating layer having a plurality of vias. Therefore, the Examiner has treated the claims as being dependent from base claim 23.

Claim Rejections - 35 USC § 112

Claims 5 and 27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 5 and 27 contain the trademark/trade name NanoBlock. Where a trademark or trade name is used in a claim as a limitation to identify or describe a particular material or

product, the claim does not comply with the requirements of 35 U.S.C. 112, second paragraph. See Ex parte Simpson, 218 USPQ 1020 (Bd. App. 1982). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. A trademark or trade name is used to identify a source of goods, and not the goods themselves. Thus, a trademark or trade name does not identify or describe the goods associated with the trademark or trade name. In the present case, the trademark/trade name is used to describe the plurality of functional blocks and, accordingly, the description is indefinite.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 6-8, 12-19, 23-25, 28-30 and 34-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Swirbel et al. (US 6,091,194).

Regarding claims 1-2, Swirbel teaches a manufacturing method for a display that includes coupling a frontplane to a backplane wherein a frontplane is top surface laminates to a backplane top surface, wherein the backplane and frontplane are fabricated separately. The frontplane includes a frontplane substrate 30 and the backplane includes a backplane substrate 20 (see Fig. 2). A transparent first electrode 32 is disposed over the frontplane substrate 30. A display medium 40 which produces electro-optical effects upon a voltage application is disposed over the first electrode 32. The device further includes a second electrode 22 that is patterned and includes a plurality of connecting regions. The backplane is electrically active to provide

driving signals for driving the pixel images, and includes a plurality of output pads on the driving circuits (transistors 24) to match the plurality of connecting regions of the second electrode 22 (col. 4, lines 9-14). Swirbel teaches that the cathode layer 22 is laminated on the backplane substrate 20 rather than being disposed over said display medium of the frontplane substrate.

It is noted that the applicant's specific intermediate location of the cathode layer, does not solve any of the stated problems or yield any unexpected result that is not within the scope of the teachings applied. Therefore it is considered to be a matter of choice, which a person of ordinary skill in the art would have found obvious to select either substrate (backplane or frontplane) to deposit the cathode layer as long as the display medium is positioned between the anode and cathode electrodes and the cathode is electrically connected to driving circuits in the final product.

Regarding claim 3, Swirbel teaches the backplane being an active matrix array of diodes (col. 2, lines 53-59).

Regarding claims 6-8, the display medium is a solid film organic electro-luminescent polymer (col. 4, lines 57-60).

Regarding claims 12-13 and 15, Swirbel teaches the first electrode 32 is made of ITO which is a transparent conductive material and has a high work function (col. 5, lines 9-12).

Regarding claims 14 and 16, Swirbel teaches the second electrode being made of aluminum which has a low work function (col. 3, lines 23-28).

Regarding claim 17, Swirbel teaches the frontplane substrate made of glass (col. 3, lines 43-45).

Regarding claim 18, Swirbel teaches the backplane substrate being made of a ceramic (col. 3, lines 10-12).

Regarding claim 19, Swirbel teaches that the backplane substrate may be formed of a flexible or rigid substrate (col. 3, lines 9-16).

Regarding claims 23-24, Swirbel teaches a display structure that includes a front plane coupled to a backplane wherein a frontplane top surface laminates to a backplane top surface, wherein the backplane and frontplane are fabricated separately. The frontplane includes a frontplane substrate 30 and the backplane includes a backplane substrate 20 (see Fig. 2). A transparent first electrode 32 is disposed over the frontplane substrate 30. A display medium 40 that produces electro-optical effects upon a voltage application is disposed over the first electrode 32. The device further includes a second electrode 22 that is patterned and includes a plurality of connecting regions. The backplane is electrically active to provide driving signals for driving the pixel images, and includes a plurality of output pads on the driving circuits (transistors 24) to match the plurality of connecting regions of the second electrode 22 (col. 4, lines 9-14). Swirbel teaches that the cathode layer 22 is laminated on the backplane substrate 20 rather than being disposed over said display medium of the frontplane substrate.

It is noted that the applicant's specific intermediate location of the cathode layer, does not solve any of the stated problems or yield any unexpected result that is not within the scope of the teachings applied. Therefore it is considered to be a matter of choice, which a person of ordinary skill in the art would have found obvious to select either substrate (backplane or frontplane) to deposit the cathode layer as long as the display medium is positioned between the anode and

cathode electrodes and the cathode is electrically connected to driving circuits in the final product.

Regarding claim 25, Swirbel teaches the backplane being an active matrix array of diodes (col. 2, lines 53-59).

Regarding claims 28-30, the display medium is a solid film organic electro-luminescent polymer (col. 4, lines 57-60).

Regarding claims 34-36, Swirbel teaches the first electrode 32 is made of ITO which is a transparent conductive material and has a high work function (col. 5, lines 9-12).

Regarding claims 37-38, Swirbel teaches the second electrode being made of aluminum which has a low work function (col. 3, lines 23-28).

Regarding claim 39, Swirbel teaches the frontplane substrate made of glass (col. 3, lines 43-45).

Regarding claim 40, Swirbel teaches the backplane substrate being made of a ceramic (col. 3, lines 10-12).

Regarding claim 41, Swirbel teaches that the backplane substrate may be formed of a flexible or rigid substrate (col. 3, lines 9-16).

Claims 4 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Swirbel et al. (US 6,091,194) in view of Smith (US 6,291,896).

Regarding claim 4, Swirbel does not specifically teach a plurality of functional blocks as the drive circuits of the backplane substrate. However, Smith teaches the use of functional blocks for driving display devices (see col. 4, lines 14-25). Smith teaches that the functional blocks can be tested before assembly so that any defective elements can be discarded before

being mounted in an array onto the substrate (col. 4, lines 35-48). This allows for a cost-effective, efficient and practical method for producing large arrays of electronic elements. Accordingly, one of ordinary skill in the art at the time the invention was made would have found it obvious to use the functional blocks taught by Smith instead of the switching means taught by Swirbel so as to reduce manufacturing costs and to ensure the quality of the individual electronic components of the array.

Regarding claim 26, Swirbel does not specifically teach a plurality of functional blocks as the drive circuits of the backplane substrate. However, Smith teaches the use of functional blocks for driving display devices (see col. 4, lines 14-25). Smith teaches that the functional blocks can be tested before assembly so that any defective elements can be discarded before being mounted in an array onto the substrate (col. 4, lines 35-48). This allows for a cost-effective, efficient and practical method for producing large arrays of electronic elements. Accordingly, one of ordinary skill in the art at the time the invention was made would have found it obvious to use the functional blocks taught by Smith instead of the switching means taught by Swirbel so as to reduce manufacturing costs and to ensure the quality of the individual electronic components of the array.

Claims 9 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Swirbel et al. (US 6,091,194) in view of Yamada (US 6,246,179).

Regarding claim 9, Swirbel does not specifically teach an insulation layer with a plurality of vias covering the output pads. However, the use of an insulation layer with a plurality of vias or contact holes is well known in the art as evidenced by Yamada. Such insulation layers provide a planar surface that allows for a secure connection of the subsequent layer, in this case

the cathode layer. The insulation layer also helps prevent short circuits from occurring while the contact holes allow for appropriate connection between parts, in this case the wiring (output pads) to the cathode layer. Accordingly, one of ordinary skill in the art at the time of the invention would have found it obvious to include an insulation layer with a plurality of vias to improve the integrity of the device.

Regarding claim 31, Swirbel does not specifically teach an insulation layer with a plurality of vias covering the output pads. However, the use of an insulation layer with a plurality of vias or contact holes is well known in the art as evidenced by Yamada. Such insulation layers provide a planar surface that allows for a secure connection of the subsequent layer, in this case the cathode layer. The insulation layer also helps prevent short circuits from occurring while the contact holes allow for appropriate connection between parts, in this case the wiring (output pads) to the cathode layer. Accordingly, one of ordinary skill in the art at the time of the invention would have found it obvious to include an insulation layer with a plurality of vias to improve the integrity of the device.

Claims 11 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Swirbel et al. (US 6,091,194) in view of Tang et al. (US 5,409,783).

Regarding claim 11, Swirbel does not specifically teach the second electrode layer being transparent. However, Tang teaches that the second electrode (cathode electrode) can be transparent so to permit light emission through the cathode (col. 5, lines 57-65). Accordingly, one of ordinary skill in the art at the time of the invention was made would have found it obvious to make the cathode electrode from a transparent material so as to permit light emission through the cathode.

Regarding claim 33, Swirbel does not specifically teach the second electrode layer being transparent. However, Tang teaches that the second electrode (cathode electrode) can be transparent so to permit light emission through the cathode (col. 5, lines 57-65). Accordingly, one of ordinary skill in the art at the time of the invention was made would have found it obvious to make the cathode electrode from a transparent material so as to permit light emission through the cathode.

Claims 20-21 and 42-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Swirbel et al. (US 6,091,194) in view of Difrancesco (US 5,670,251).

Regarding claims 20-21, Swirbel does not specifically teach the use of a pressure sensitive adhesive that consists of conducting and nonconducting regions to connect the backplane to the frontplane. However, Difrancesco teaches treating a pressure sensitive conductor layer by patterning the layer so that it includes conducting and nonconducting regions (see abstract). Difrancesco teaches that using such an adhesive allows for substrates to be mechanically and electrically connected where desired (such as between the output pads and the connecting regions of the cathode electrode) and electrically isolated where desired (such as between adjacent output pads). Accordingly, one of ordinary skill in the art at the time of the invention would have found it obvious to coat a pressure sensitive conductive layer over the output pads of the backplane substrate and patterning the layer such that it consists of conducting and nonconducting regions wherein the conducting regions match with the connecting regions and the output pads in order to mechanically and electrically connect the two substrates while preventing short-circuits from occurring in the device.

Rejection of claim 1 applies.

Regarding claims 42-43, Swirbel does not specifically teach the use of a pressure sensitive adhesive that consists of conducting and nonconducting regions to connect the backplane to the frontplane. However, Difrancesco teaches treating a pressure sensitive conductor layer by patterning the layer so that it includes conducting and nonconducting regions (see abstract). Difrancesco teaches that using such an adhesive allows for substrates to be mechanically and electrically connected where desired (such as between the output pads and the connecting regions of the cathode electrode) and electrically isolated where desired (such as between adjacent output pads). Accordingly, one of ordinary skill in the art at the time of the invention would have found it obvious to coat a pressure sensitive conductive layer over the output pads of the backplane substrate and patterning the layer such that it consists of conducting and nonconducting regions wherein the conducting regions match with the connecting regions and the output pads in order to mechanically and electrically connect the two substrates while preventing short-circuits from occurring in the device.

Rejection of claim 23 applies.

Claims 20, 22, 42, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Swirbel et al. (US 6,091,194) in view of Miyamoto et al. (US 6,039,896).

Regarding claims 20 and 22, Swirbel does not specifically teach the use of a pressure sensitive adhesive that consists of conducting and nonconducting regions to connect the backplane to the frontplane. However, Miyamoto teaches an anisotropic conductive adhesive used to mechanically and electrically connect electrical components. Miyamoto teaches that such anisotropic conductive adhesive is a z-direction conductive film that allows conductivity only in a perpendicular direction to a top and bottom surface (col. 1, lines 15-32). Accordingly,

one of ordinary skill in the art at the time of the invention would have found it obvious to coat such an anisotropic conductive adhesive layer over the output pads in order to connect the backplane substrate to the frontplane substrate so as to electrically connect the output pads to the corresponding connecting regions of the cathode layer while electrically insulating the areas between adjacent output pads and adjacent pixel electrodes preventing the occurrence of short-circuits in the device.

Rejection of claim 1, applies.

Regarding claims 42 and 44, Swirbel does not specifically teach the use of a pressure sensitive adhesive that consists of conducting and nonconducting regions to connect the backplane to the frontplane. However, Miyamoto teaches an anisotropic conductive adhesive used to mechanically and electrically connect electrical components. Miyamoto teaches that such anisotropic conductive adhesive is a z-direction conductive film that allows conductivity only in a perpendicular direction to a top and bottom surface (col. 1, lines 15-32). Accordingly, one of ordinary skill in the art at the time of the invention would have found it obvious to coat such an anisotropic conductive adhesive layer over the output pads in order to connect the backplane substrate to the frontplane substrate so as to electrically connect the output pads to the corresponding connecting regions of the cathode layer while electrically insulating the areas between adjacent output pads and adjacent pixel electrodes preventing the occurrence of short-circuits in the device.

Rejection of claim 23, applies.

Allowable Subject Matter

Claims 10 and 32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

the references of the Prior Art of record fails to teach or suggest the combination of the limitations as set forth in claims 10 and 32, and specifically comprising the limitation of conductive adhesives formed over the plurality of vias in the insulating layer.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Shimoda et al. (US 2002/0158577 A1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to *Anthony Perry* whose telephone number is (703) 305-1799. The examiner can normally be reached between the hours of 9:00AM to 5:30PM Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel, can be reached on (703) 305-4794. The fax phone number for this Group is (703) 308-7382.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [**Anthony.perry@uspto.gov**].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Anthony Perry
Patent Examiner
Art Unit 2879
September 24, 2003

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